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September 12, 2005

TO: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Attn: Art Unit 2827 - Examiner David A Zarneke

FROM: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

SUBJECT: Serial #: 09/837,007
File Date: April 18, 2002
Inventor: M.S. Lin, et al.
Examiner: David A Zarneke
Art Unit: 2827
Title: A Structure and Manufacturing Method of a Chip Scale
Package

RESPONSE TO COMMUNICATION

Dear Sir:

This is in response to the PTO communication dated Aug. 10, 2005.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on Sept. 12, 2005.

Signature 
Stephen B. Ackerman, Reg. No. 37,761

Date: Sept. 12, 2005

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 6 of this paper.